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For the Patent- and Registration Office

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METHOD AND APPARATUS FOR PROVIDING ROUTING IN A CIRCUIT SWITCHED NETWORK

Technical Field of Invention

The present invention refers to a method and an apparatus for providing routing of asynchronous traffic in a circuit switched synchronous time division multiplexed network, more specifically in a DTM network.

Background of the invention

Today, new types of circuit-switched communication networks are being developed for the transfer of information using synchronous time division multiplexed bitstreams. Within this field, a new technology, referred DTM (Dynamic synchronous Transfer Mode), are currently being developed, primarily addressing the problem of providing quality of service to users of real-time, broadband applications.

The structure of a DTM network has been described in, e.g., "The DTM Gigabit Network", Christer Bohm, Per Lindgren, Lars Ramfelt, and Peter Sjödin, Journal of High Speed Networks, 3(2):109-126, 1994, and in "Multi-gigabit networking based on DTM", Lars Gauffin, Lars Håkansson, and Björn Pehrson, Computer networks and ISDN Systems, 24(2):119-139, April 1992.

The basic topology of a DTM network is preferably a bus with two unidirectional, multi-access, multi-channel optical fibers connecting a number of nodes, each node being arranged to serve one or more end users connected thereto. However, the topology may just as well be any other kind of structures e.g. a ring structure or a hub structure.

The bandwidth of each wavelength on the bus, i.e. each bitstream on each fiber, is divided into recurrent fixed length frames, which in turn are divided into fixed size time slots. The number of slots in a frame thus depends on the network's bit-rate. The time slots are

divided into two groups, control slots and data slots. Control slots are typically used for transferring of signaling messages between said nodes for the network's internal operation. The data slots are typically used for the transfer of data between end users connected to the different nodes.

Each node is arranged to dynamically establish, terminate, and modify DTM channels by dynamically allocating time slots thereto.

When DTM channels are used for transferring asynchronous traffic, such as TCP/IP packets, a mechanism for providing routing of said packets through the DTM network is needed. However, current available routing solutions are typically developed for use in other kinds of network architectures and therefore suggest mechanism that results in poor use of the advantageous aspects of a network of the DTM kind.

It is therefore an object of the invention to provide a routing solution in a network of the DTM kind, which make better use of the features of such a network.

Summary of the Invention

The above mentioned and other objects are achieved by the invention as defined in the accompanying claims.

Hence, according to the invention, a multi-channel multi-access bitstream carrying isochronous channels is accessed, said isochronous channel being used for the transfer of asynchronous traffic, and a data packet from a node connected to said bitstream is received in an isochronous channel thereof. Then, it is determined if said data packet is to be transmitted to another node connected to said bitstream using another channel of said isochronous channels. If so, said data packet is transmitted to said another node using said another channel of said isochronous channels on said bitstream.

The invention thus provides routing of data packets among isochronous channels of one and the same multi-

channel multi-access bitstream. Typically, in conventional solutions, a router is provided to interconnect two or more separate networks or, network sections, and to provide routing of data packets between such network sections. The routing solution according to the invention differs from this conventional approach in that routing is provided within one single network section, more specifically among the channels of a multi-channel multi-access bitstream. Consequently, a routing mechanism according to the invention, providing routing among channels of a single bitstream, need not be provided at an exit point of the bitstream, i.e. at the point of interconnection, typically via a switch or the like, to another bitstream. Note, however, that this does not mean that a routing mechanism according to the invention is limited to routing with respect to channels of one single bitstream only, as one may use conventional routing from said bitstream to another bitstream as well without departing from the scope of the invention.

As is understood, the routing mechanism according to the invention provides the network designer with a greater freedom of architecture when designing networks. An example thereof will be described below with reference to Fig. 5.

According to a preferred embodiment of the invention, channels of said bitstream that are not to be routed by said routing mechanism are not accessed by said routing mechanism. Instead, such channels are bypassed, typically at the interface of an apparatus providing said routing mechanism. Consequently, the traffic in said bypassed channels will be unattended and unaffected by said routing mechanism. Of course, this requires the provision of means for separating channels of said isochronous channels that are to be received and channels that are not to be received.

However, according to an embodiment of the invention, if a data packet is received in a channel which

carries asynchronous traffic that is to be routed by the routing apparatus but however also extends beyond the routing apparatus, i.e. a mulicasted channel that isn't set to terminate at the routing apparatus, further propagation of said data packet to other nodes connected to said bitstream using the isochronous channel from which said data packet was received is uninhibited. Consequently, as an example, a channel may be a multicast channel ~~wherein a data packet will reach a set of receivers, but~~ wherein said data packet will at the same time be routed to another channel of said bitstream, for example to reach another set of receivers.

As mentioned in the introduction, a preferred use of the invention is in a network operating according to a Dynamic synchronous Transfer Mode (DTM) protocol, i.e. a so called DTM network, said isochronous channels then being DTM channels in said DTM network.

For definition, as referred to herein, a "DTM network" is a circuit switched time division multiplexed network of the kind wherein information is transferred between nodes of the network on bitstreams. Each bitstream is divided into regularly recurrent, fixed size frames, so called DTM frames, each comprising a number of fixed size time slots, said time slots being separated into control slots and data slots. Thus, at each given point in time, a time slot position of a DTM frame defines either a control slot or a data slot. Control slots are used for control signaling between nodes of the network, and data slots are used for the transfer of user data (sometimes often referred to as payload data).

Furthermore, in a DTM network, write access to the time slots of a DTM frame is distributed among nodes ~~being attached to the bitstream carrying said DTM frame,~~ each node typically having write access to a respective at least one control slot and a respective dynamically adjustable set of data slots within each recurrent frame.

Moreover, having write access to a time slot position in a frame means having write access to said time slot position within each recurrent frame.

In a DTM network, a node will use the data slots it has write access to for establishing so called DTM channels by allocating one or more of said data slots to each respective DTM channel. Hence, as referred to herein, a DTM channel is defined by one or more time slots occupying the same time slot position within each DTM frame of the bitstream upon which said DTM channel is carried. However, if a DTM channel reaches, for example, over two bitstreams, the channel may of course be defined by a different set of time slot positions on the two bitstreams. Also, a DTM channel may be either a control channel or a data channel, depending on whether control or data slots that is allocated to said channel. Furthermore, a DTM channel may be unicast, multicast or broadcast.

As the demand for network capacity changes, DTM channels may be dynamically established, terminated, or modified, the latter by changing the number of time slots allocated to a DTM channel. Also, the distribution of write access to time slot among different nodes may be dynamically modified as different nodes develop different needs for control signaling and data transfer.

According to another preferred embodiment of the invention, a routing mechanism according of the above mentioned kind is performed in relation to a memory which provides temporary storing of data packets at memory locations thereof, said memory locations being temporarily allocated for storing respective data packets. Said memory is then accessed for storing/transmission of data packets irrespective of which channel a data packet is received upon/transmitted into, and is thus used as a shared memory shared by all channels. This will provide a comparatively simple design for managing data packets in

relation to multi-channel routing according to the invention.

Further aspects and advantages of the invention will be more fully understood by those skilled in the art from the accompanying claims and from the following detailed description of exemplifying embodiments thereof.

Brief Description of the Drawings

Exemplifying embodiments of the invention will now be described with reference to the accompanying drawings, wherein:

Fig. 1 schematically shows en example of the structure of a bitstream in a circuit switched time division multiplexed network operating according to a DTM protocol;

Fig. 2 schematically illustrates transfer of asynchronous traffic in one of the isochronous channels carried by the bitstream shown in Fig. 1;

Fig. 3 schematically shows an exemplifying embodiment of an apparatus according to the invention;

Fig. 4 schematically shows another exemplifying embodiment of an apparatus according to the invention; and

Fig. 5 schematically shows a network comprising the apparatus shown in Fig 4.

Detailed Description of an Exemplifying Embodiment

An example of the structure of a multi-channel multi-access bitstream B in a circuit switched time division multiplexed network operating according to a DTM protocol will now be described with reference to Fig. 1.

As shown in Fig. 1, the bitstream B is divided into recurrent, essentially fixed sized frames, wherein the start of each frame is defined by a frame synchronization time slot F. Each frame will have a duration of 125 μs.

Each frame is further divided into a plurality of fixed sized, typically 64 bit, time slots. When using

said frame length of 125 μs, a time slot size of 64 bits, and a bit rate of 2Gbps, the total number of time slots within each frame will be approximately 3900.

The time slots are divided into control slots C1, C2, C3, and C4, and data slots D1, D2, D3, and D4. The control slots are used for control signaling between the nodes of the network, whereas the data slots are used for the transfer of payload data. Each node connected to the bitstream B is typically allocated at least one control slot, i.e. each node will have write access to at least one control slot. Furthermore, write access to data slots are distributed among the nodes connected to the bitstream. Consequently, a node N1 (connected to the bitstream B) will have access to a control slot C1 and a set of data slots D1 within each frame of the bitstream, node N2 (also connected to the bitstream) will have access to a control slot C2 and a set of data slots D2 within each frame of the bitstream, and so on. The set of slots allocated to a node as control slot(s) and/or data slot(s) occupy the same slot position within each frame of the bitstream. Hence, in the example, the control slot C1 belonging to node N1 will occupy the second time slot within each frame of the bitstream.

During network operation, each node may increase or decrease its access to control slots and/or data slots, thereby re-distributing the access to control slots and/or data slots among the nodes. For example, a node having a low transfer capacity demand may give away its access to data slots to a node having a higher transfer capacity demand. Furthermore, the slots allocated to a node need not be consecutive slots, but may reside anywhere within the frame.

Also, note that each frame begins with said frame synchronization time slot, defining the frame rate on the bitstream, and ends with one or more guard band time slots G.

In Fig. 1 at (c), it is furthermore assumed that node N2, having access to its control slot C2 and its range of data slots D2, has established four channels CH1, CH2, CH3, and CH4 on the bitstream. As shown, each channel is allocated a respective set of slots. In the example, the transfer capacity of channel CH1 is larger than the transfer capacity of channel 2, since the number of time slots allocated to channel CH1 is larger than the number of time slots allocated to channel CH2. The time slots allocated to a channel occupy the same time slot positions within each recurrent frame of the bitstream.

An example of the transfer of asynchronous traffic in one of the isochronous channels carried by the bitstream B shown in Fig. 1 will now be described with reference to Fig. 2. In Fig. 2, it is assumed that the channel CH3 shown in Fig. 1 is established to carry asynchronous traffic in the form of sequentially transmitted variable size data packets, which for example could be TCP/IP packets of Ethernet frames. (Note that Fig. 2 only shows the sequence of time slots transmitted within the channel CH3). Since Fig. 1 schematically indicates that channel CH3 comprises seven time slots within each frame on bitstream B, the first seven time slots transmitted in the channel CH3, i.e. the first seven time slots in Fig. 2, will be transmitted in one frame, the next seven time slots will be transmitted in the next frame, and so on.

Fig. 2 shows three data packets transmitted in channel CH3. Each data packet is encapsulated according to a predefined encapsulation protocol. In Fig. 2, it is assumed that the encapsulation protocol defines that each data packet shall be divided into a number of 64 bit data blocks (corresponding to the size of a time slot), that a start_of_packet slot S is to be added to the start of each data packet, and that an end_of_packet slot E is to be added to the end of each data packet, thereby forming encapsulated data packets P1, P2, and P3. In case of gaps

between packets, the bitstream is provided with so called idle slots, identifying said gaps as not providing valid data.

An embodiment of an apparatus according to the invention will now be described with reference to Fig. 3. In Fig. 3, the apparatus 110 comprises a port 111, which in turn comprises an incoming channel interface 113 and an outgoing channel interface 114 providing read and write access, respectively, to a bitstream B, which for example may be the bitstream B shown in Fig. 1. The incoming and outgoing channel interface will provide for synchronization of the operation of the apparatus in relation to the frame and slot rate on the bitstream B.

The incoming channel interface and the outgoing channel interface are connected to an incoming channel manager 115 and an outgoing channel manager 116, respectively. The incoming channel manager 115 and the outgoing channel manager 116 are both connected to a routing processor 117, a shared memory 119, a buffer manager 120, and a control unit 121. The routing processor 117 is in turn connected to a routing memory 118.

In operation, the incoming channel interface 113 will receive (arrow 1) data packets from the channels monitored by said interface, such as the encapsulated TCP/IP packets on channel CH3 as shown in Fig. 2. Each data packet is encapsulated according to a predefined protocol and will typically be received as a set of consecutive sequential 64 bit data blocks.

The incoming channel interface 113 will then forward, with preserved sequential order, each received data block to the incoming channel manager 115 (arrow 2). Each data block forwarded to the incoming channel manager 115 is accompanied by a channel identifier, designating the channel from which it was received.

Having received sufficiently many data blocks at the head end of a data packet to be able to derive information designating the size of the data packet, the

incoming channel manager will send a request (arrow 3), containing the size of the data packet, to the buffer manager 120. The request will thereby inform the buffer manager 120 that the incoming channel manager 115 needs to store a data packet of the designated size in the shared memory 119.

The buffer manager 120 will then allocate an address space of the shared memory 119 to said data packet, the size of the allocated address space not being smaller than the size of said data packet. The buffer manager 120 will answer the request by returning (arrow 4) a start address corresponding to the start of said address space to the incoming channel manager 115.

Having received said start address from the buffer manager 120, the incoming channel manager will start writing the data blocks forming the associated data packet into the shared memory 119 (arrow 5), starting at the start address received from the buffer manager 120 and incrementing the address one step for each data block written into the shared memory 119.

At the same time, the incoming channel manager 115 will send the start address received from the buffer manager 120, along with the IP address designated in the header of the data packet, to the routing processor 117 (arrow 6).

Using the routing memory 118 (arrow 7), the routing processor will, based upon the destination address received from the incoming channel interface 115, determine whether or not the associated data packet is to be transmitted from the outgoing channel interface 114 and, if so, which outgoing channel that is to be used when transmitting said data packet.

Having determined an outgoing channel for the data packet, the routing processor 117 will transmit a signal to the outgoing channel manager 116 (arrow 8), containing a channel identifier and the start address received from the incoming channel manager. The channel identifier

identifies the outgoing channel to be used when transmitting the associated data packet address, and the start address designates where to read the associated data packet from in the shared memory 120.

Having received the outgoing channel identifier and the start address from the routing processor 117, the outgoing channel manager 116 will access the shared memory (arrow 9) and start reading (arrow 10) data blocks forming the associated data packet from the shared memory 119, beginning at the start address received from the routing processor 117 and incrementing the address one step for each data block read from the shared memory 119.

At the same time, the outgoing channel manager 116 will continuously receive requests (arrow 11) for data blocks for respective outgoing channels from the outgoing channel interface 114, said request being sent from the outgoing channel interface at the rate as time slots allocated to the respective channel passes on the outgoing bitstream accessed via the outgoing channel interface 114.

As triggered by said requests for data blocks, when said requests relates to a channel identified by the a channel identifier received form the routing processor 117, the outgoing channel manager 116 will forward (arrow 12), with preserved sequential order, each data block of the associated data packet, as read from the shared memory 119 starting at the designated start address, to the outgoing channel interface 114. The outgoing channel interface 114 will then, in turn, forward (arrow 13) the received data blocks to the respective channels on the outgoing bitstream.

Having read the last data block of a data packet from the shared memory 119, the outgoing channel manager 120 will return (arrow 14) the associated start address, which was received from the routing processor 117, to the buffer manager 120. This will inform the buffer manager that the processing of the data packet stored at the

address space associated with said start address is complete and that the buffer manager is now free to allocate said address space to a new data packet received via the incoming channel interface.

Furthermore, the control unit 121 will determine which channels that are to be received by the incoming channel interface 113, which will typically be those channels use for transmission of data packets that need routing by the routing processor 117. Channels that are not to be directed to the routing processor 117, as determined by the control unit 121, are bypassed at the incoming/outgoing channel interface 113, 114 and are consequently not processed by the routing processor.

Another embodiment of an apparatus according to the invention will now be described with reference to Fig. 4. In the apparatus shown in Fig. 4, the only difference compared to the embodiment shown in Fig. 3 is that, in Fig. 4, the incoming channel manager 115 is provided with a cache memory 122. The cache memory 122 contains a list of destination addresses for which no routing is needed by the routing processor 117, as previously determined by the routing processor. A received data packet referring to an address among said list of destination addresses shall not be directed to the routing processor 117. The routing processor will continuously update the content of the cache memory 122.

Consequently, when receiving a data packet, the incoming channel manager 115 will compare the destination address of the data packet against the destination addresses contained in the cache memory 122. If a match is found, the data packet will be discarded at the incoming channel manager and will hence not be directed to the routing processor 117, thereby decreasing the processing load on the routing processor 117.

(Note, however, that if the channel from which said data packet was received does not terminate at the apparatus 110 but instead continuos to one or more other

downstream nodes, e.g. if the channel is a multicast or broadcast channel, the data packet will be forwarded to downstream nodes in the same channel as it was received irrespective of whether or not it is discarded at the incoming channel manager. Whether or not this bypassing is done at the incoming/outgoing channel interfaces 113, 114 or at the incoming/outgoing channel managers 115, 116 will typically be determined by the control unit 121).

A network utilizing the invention will now be described with reference to Fig. 5. In Fig. 5, an multi-channel multi-access bitstream B, which for example may be the bitstream B shown in the previous figures, forms a closed loop link connecting a plurality of access nodes A using circuit switched time division multiplexing according to a DTM protocol. A switch node S connected to the link provides connectivity between said link and another link that also uses circuit switched time division multiplexing according to said DTM protocol. On the latter link, a router R provides access to a packet switched network, such as the Internet. Furthermore, an apparatus 110 according to the invention, e.g. the apparatus described with reference to Fig. 3 or Fig. 4, is connected to the bitstream B.

In Fig. 5, the node apparatus 110 will typically have established an isochronous channel to the router R via the switch S. When an end user attached to an access node A on the bitstream B wants to send a data packet, it may establish a channel to the appropriate destination on its own decision, for example a channel to another access node on the bitstream B or a channel to the router R via the switch S. However, it may also use a channel to the node apparatus 110, which will then, having received the data packet, see to that the data packet is forwarded to the appropriate destination, for example via a channel to the router R.

According to an alternative embodiment, multicast channels are established from each node connected to the

bitstream B to all other nodes connected to the bitstream B. If an end user attached to an access node A on the bitstream B wants to send a data packet to any destination, it will then simply multicast the packet using said multicast channel. As the multicasted packet is read at the nodes receiving said multicast channel, if it turns out that the destination address of the data packet refers to an end user connected to another access node on said bitstream, said another node will see to that the data packet is forwarded to said end user. However, if it turns out that the destination address of the data packet refers to an end user not connected to via an access node to said bitstream, the node apparatus 110 will see to that the data packet is forwarded to the appropriate destination, for example via a point-to-point channel to the router R.

Even though the invention has been described above with reference to exemplifying embodiments thereof, these are not to be considered as limiting the scope of the invention. Consequently, as understood by those skilled in the art, different modifications, combinations and alterations may be made within the scope of the invention, which is defined by the accompanying claims.

CLAIMS

1. A method for providing routing of asynchronous traffic in a circuit switched synchronous time division multiplexed network, said method comprising the steps of:

receiving, in an isochronous channel of a multi-channel multi-access bitstream carrying isochronous channels, said isochronous channel being used for the transfer of asynchronous traffic, a data packet from a node connected to said bitstream;

determining if said data packet is to be transmitted to another node connected to said bitstream using another channel of said isochronous channels; and, if so,

transmitting said data packet to said another node using said another channel of said isochronous channels on said bitstream.

2. A method as claimed in claim 1, comprising the steps of determining which channels of said isochronous channels that are to be received and bypassing those channels that are not to be received.

3. A method as claimed in claim 1 or 2, comprising the step of discarding said data packet if said data packet is not to be transmitted to another node connected to said bitstream using another channel of said isochronous channels.

4. A method as claimed in claim 1, 2, or 3, wherein further propagation of said data packet to other nodes connected to said bitstream using the isochronous channel from which said data packet was received is uninhibited.

5. A method as claimed in claim 1, 2, 3, or 4, wherein said data packet, when transmitted within said channel, is encapsulated according to a predefined encapsulation protocol.

6. A method as claimed in any one of the preceding claims, wherein said steps are performed at a node connected to said multi-channel multi-access bitstream.

7. A method as claimed in any one of the preceding claims, wherein said steps are performed at a node which provides routing of data packets only among channels carried by said multi-channel multi-access bitstream.

8. A method as claimed in any one of the preceding claims, wherein said network is operating according to a Dynamic synchronous Transfer Mode (DTM) protocol.

9. A method as claimed in any one of the preceding claims, wherein said receiving step comprises temporarily allocating a location of a shared memory for storing said data packet and temporarily storing said data packet at said location of said shared memory, and wherein said transmitting step comprises reading said data packet from said location of said shared memory.

10. An apparatus (110) providing routing of asynchronous traffic in a circuit switched synchronous time division multiplexed network, comprising:

an interface (111) providing access to a multi--channel multi-access bitstream carrying isochronous channels; and

routing means (117) for determining if a data packet received by said interface in an isochronous channel of said isochronous channels, said isochronous channel carrying asynchronous traffic, is to be transmitted using another one of said isochronous channels and, if so, directing said data packet thereto via said interface.

11. An apparatus as claimed in claim 10, comprising means for determining which channels of said isochronous

channels that are to be received by said interface and which channels that are to be bypassed at said interface.

12. An apparatus as claimed in claim 10 or 11, wherein said interface means comprises means (122) for determining if said data packet is not to be transmitted using another one of said isochronous channels and, if so, preventing said data packet from being processed by said routing means.

13. An apparatus as claimed in claim 10, 11, or 12, wherein said interface is arranged to forward said data packet using the isochronous channel from which said data packet was received in addition to the decisions made by said determining means.

14. An apparatus as claimed in claim 10, 11, 12, or 13, wherein said data packet, when transmitted within said channel, is encapsulated according to a predefined encapsulation protocol.

15. An apparatus as claimed in any one of claims 10-14, wherein said routing means provides routing of data packets only among channels carried by said multi-channel multi-access bitstream.

16. An apparatus as claimed in any one of claims 10-15, wherein said network is operating according to a Dynamic synchronous Transfer Mode (DTM) protocol.

17. An apparatus as claimed in any one of claims 10-16, further comprising a memory (119) for temporarily storing said data packet at a memory location thereof, said memory location being temporarily allocated for storing said data packet, wherein said interface is arranged to write said data packet into said allocated memory location when receiving said data packet and to

read said data packet from said allocated memory location when transmitting said data packet.

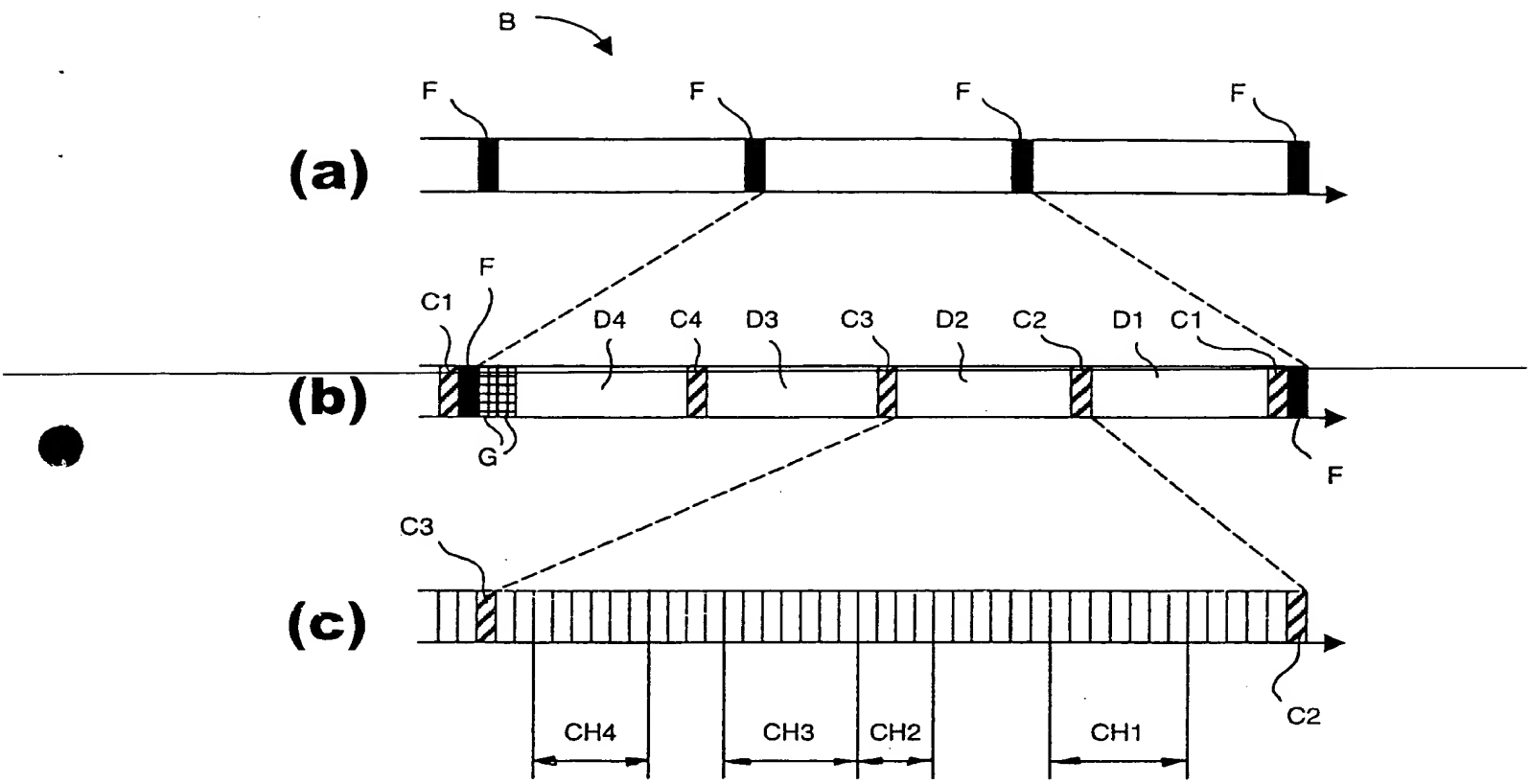
18. An apparatus as claimed in claim 17, further comprising a storage manager (120) being arranged to temporarily allocate a memory location for storing said data packet and to provide said interface with information designating said memory location for storing said data packet.

19. An apparatus as claimed in claim 17 or 18, wherein said memory location is allocated for storing said data packet as a result of a request made by said interface when receiving said data packet.

ABSTRACT

Hence, according to the invention, a multi-channel multi-access bitstream (B) carrying isochronous channels is accessed, said isochronous channel being used for the transfer of asynchronous traffic, and a data packet from a node connected to said bitstream is received in an isochronous channel thereof. Then, it is determined if said data packet is to be transmitted to another node connected to said bitstream using another channel of said isochronous channels. If so, said data packet is transmitted to said another node using said another channel of said isochronous channels on said bitstream.

Elected for publication: Fig. 3.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F
F
F
F
(a)
F
C1
D4
C4
D3
C3
D2
C2
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G
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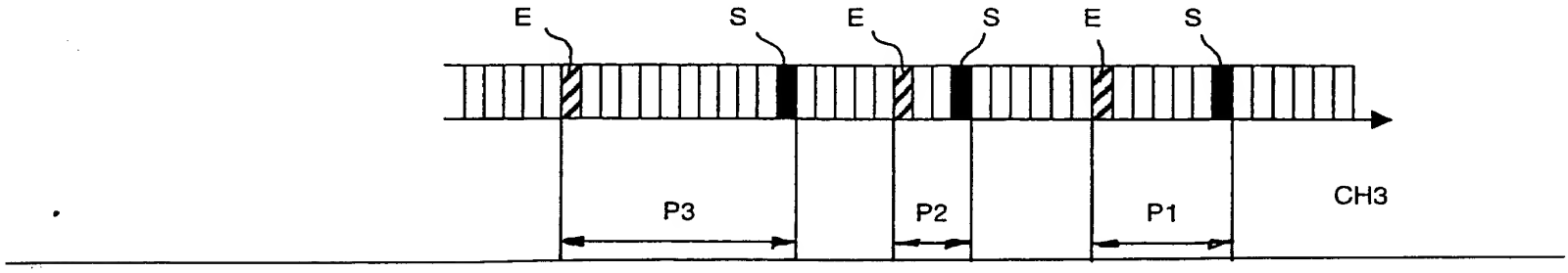
(c)
C2
CH4
CH3
CH2
CH1

Fig. 1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P3
P2
P1
CH3

Fig. 2

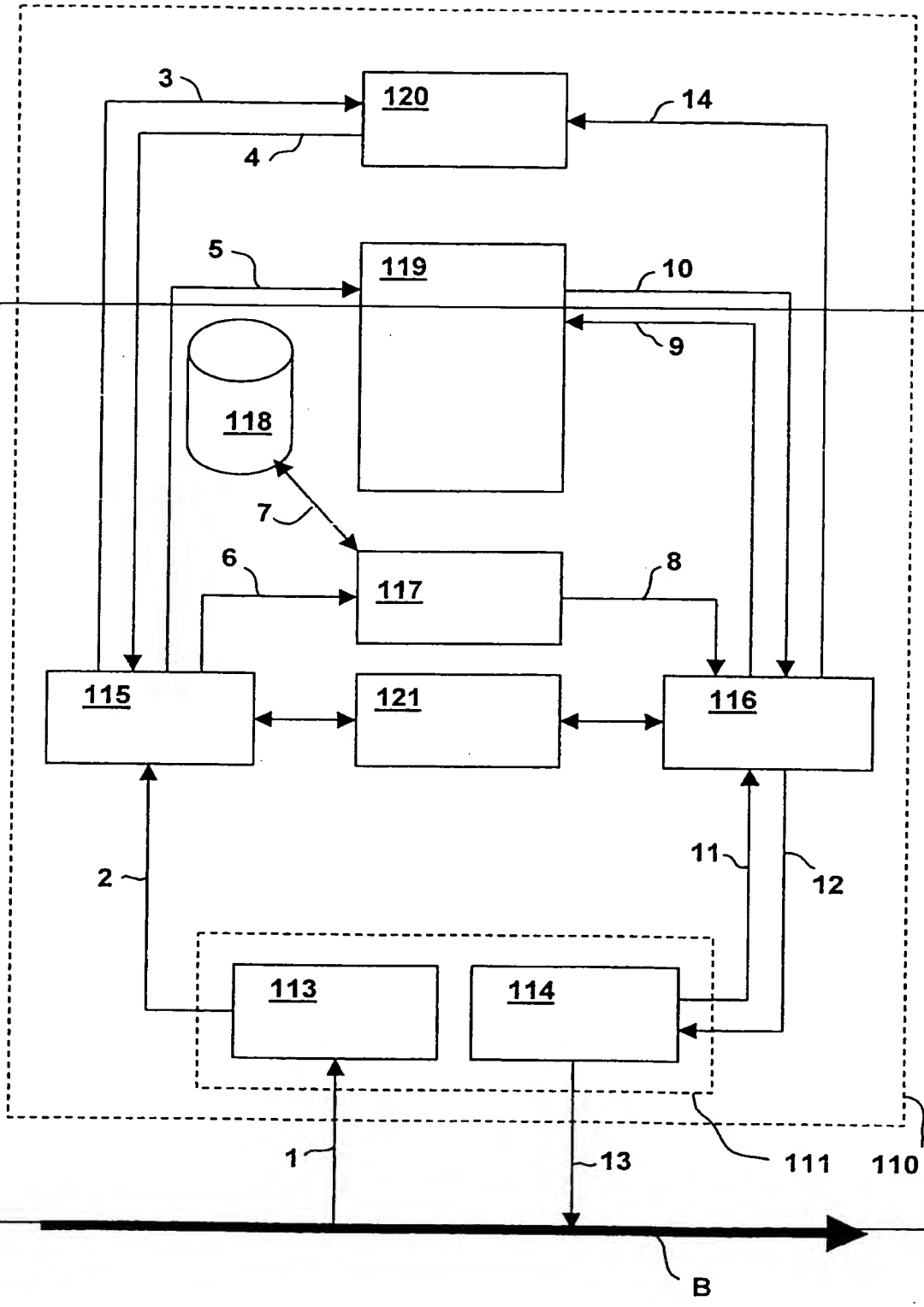
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Fig. 3

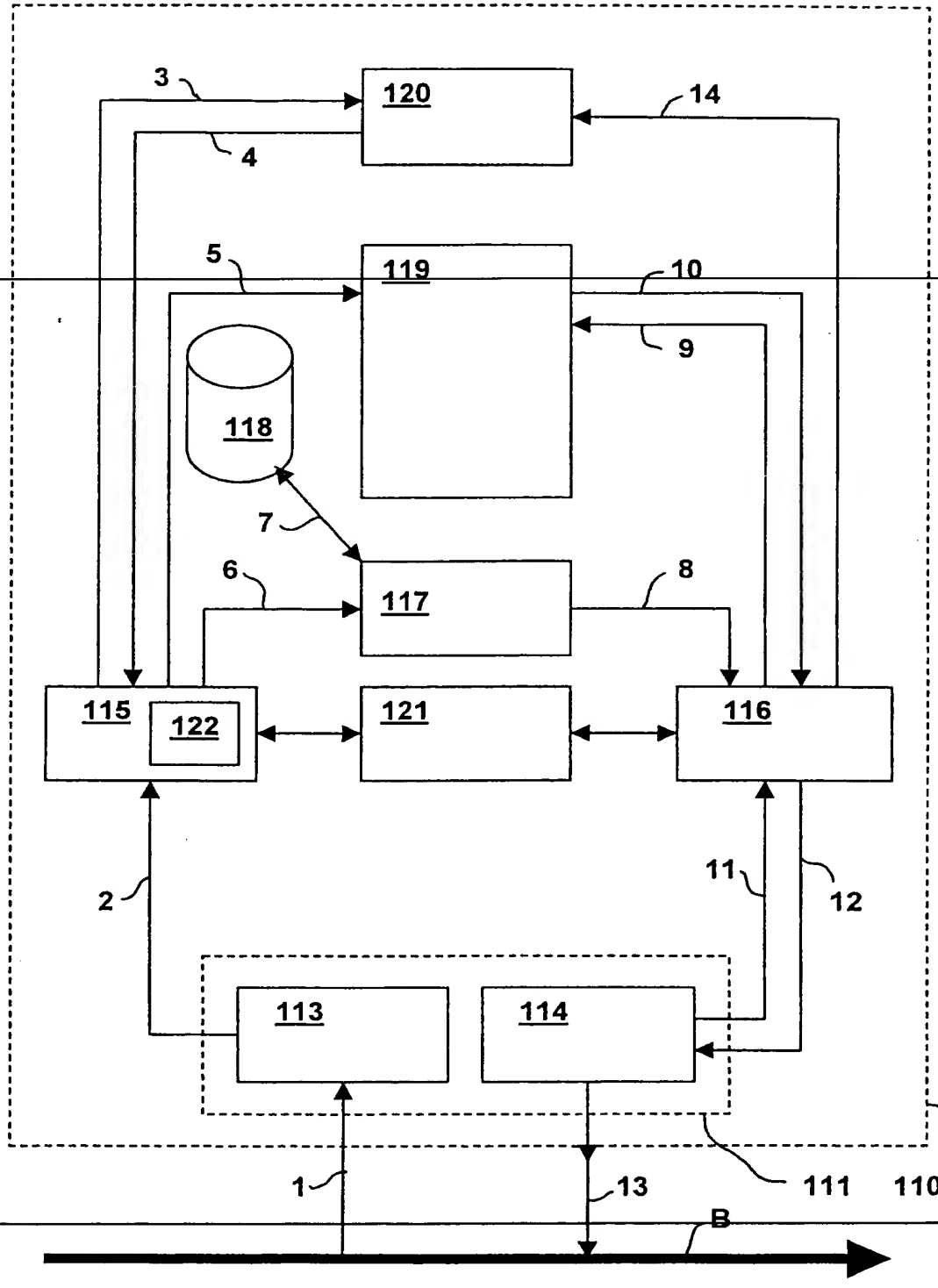
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Fig. 4

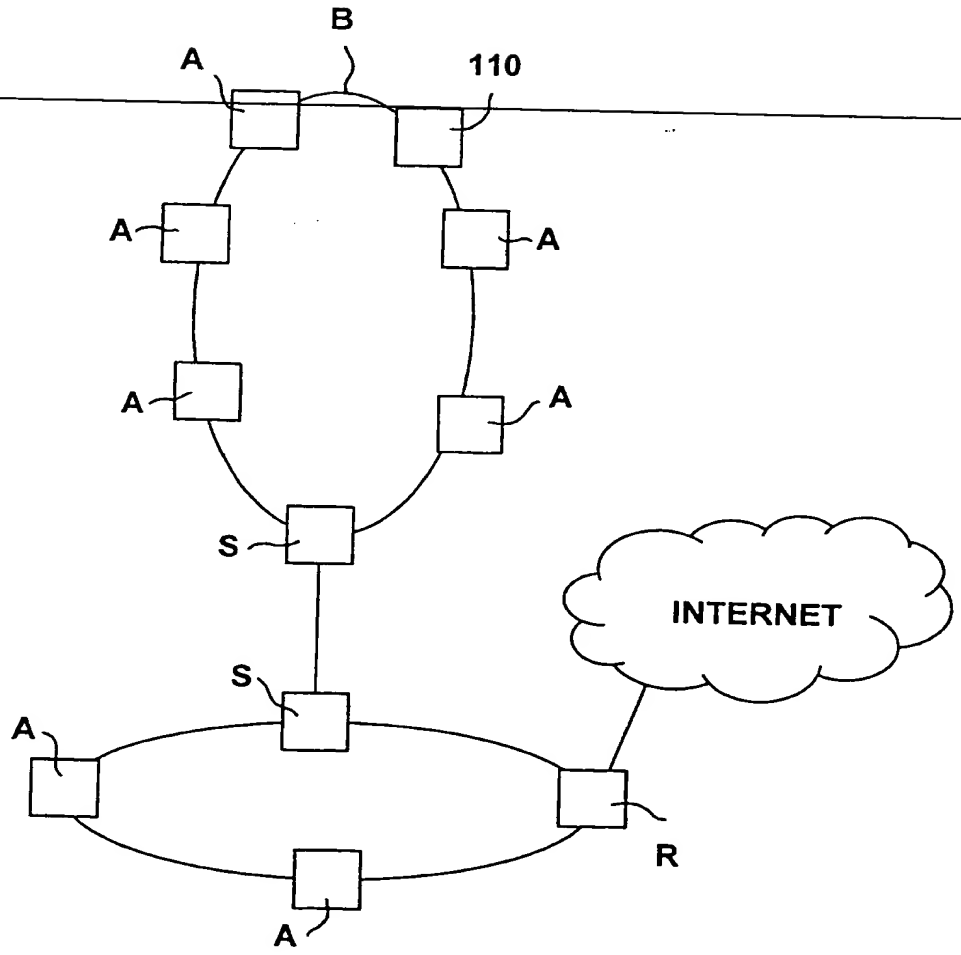

Fig. 5